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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,150	08/02/2001	Jin Chuan Bai	MM4460	7226

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EXAMINER
ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,150	BAI, JIN CHUAN	
	Examiner	Art Unit	
	David A. Zarneke	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Foreign Priority

Applicant is notified that the claim for foreign priority has now been perfected as a result of submission of a certified copy of the reference.

Response to Arguments

Applicant's arguments with respect to the rejection(s)of claim(s) 1-8 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made, which is detailed below.

Applicant first argues that the rejection of the claims over Ito in view of Urushima fail to teach the amended limitation stating that a printing technique is used to deposit the first encapsulant such that it is coplanar with the top surface of the conductive elements.

The examiner agrees with this argument and withdraws the rejection of the claims. A new rejection of the claims is presented below that covers this limitation.

A second argument is presented, but it is void since the rejection using Ito in view of Urushima has been withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Applicant's admitted prior art.

Booth teaches a direct chip attachment process comprising:

1) preparing a substrate (1) having a first surface and a second surface, wherein at least one chip-mounting area (8) is formed on the first surface;

2) disposing a plurality of conductive elements (4) on the chip-mounting area of the substrate, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant (2) by a mask screening (3, 20-21), which is a type of printing process, on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant formed by printing is adapted to have a top surface thereof formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant (Figure 9); and

4) preparing at least one semiconductor chip (6) having a plurality of bond pads (Figure 14) formed on a surface thereof and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by

the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface (Figures 5-9 & 14).

Booth fails to teach the steps 5 and 6, namely the encapsulating of the chip and the implanting of solder balls onto the opposite side of the substrate.

Applicants admitted prior art teaches that it is well known in the art to encapsulate a chip and to implant solder balls to the opposite side of the substrate (specification, page 1, 3rd paragraph).

It would have been obvious to one of ordinary skill in the art to use the chip encapsulation and solder ball implantation of Applicant's admitted prior art in the invention of Booth because these are conventional step used in the packaging of a chip.

The use of conventional materials to perform there known functions in a conventional process is obvious. *In re Raner* 134 USPQ 343 (CCPA 1962).

Regarding claim 2, Booth teaches the conductive elements as being conductive bumps (3, 1).

With respect to claim 3, while Booth teaches a conductive adhesive as the conductive element (3, 21+), tin, lead, or a tin/lead alloy conductive element is an equivalent type of conductive element that is commonly used in the art.

While Booth lists a few undesirable attributes of solder alloys, Booth does state that solder alloys are pervasively used to interconnect components to carriers (1, 22+).

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution. Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin

125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 5, Booth teaches the use of conductive metal contacts (8), aka bond pads, electrically connected to chip sites on the surface of the substrate (2, 52+).

Regarding claim 6, Booth teaches the 2nd surface of the chip as having no bond pads (Figure 14).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Applicant's admitted prior art as applied to claim 1 above, and further in view of Cook, US Patent 6,331,446.

Booth and Applicant's admitted prior art both fail to teach the 2nd encapsulant as exposing the outside surface of the chip, which has no bond pads.

Cook teaches a process of underfilling a C4 IC package comprising a 2nd encapsulant that forms a fillet around the edges of the chip without encapsulating the outer surface of the chip (Figure 3).

It would have been obvious to one of ordinary skill in the art to use the fillet of Cook in the combined invention of Booth and Applicant's admitted prior art because Cook teaches that the fillet seals the edges of the chip and the underfill such that moisture migration is inhibited and chip and/or underfill cracking is prevented (2, 56+).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Booth, US Patent 5,543,585, in view of Applicant's admitted prior art as applied to claim 1 above, and further in view of Lai, US Patent 6,323,066.

Booth and Applicant's admitted prior art both fail to teach the use of a heat sink that is encapsulated by the 2nd encapsulant.

Lai teaches a heat-dissipating structure comprising attaching a chip to a substrate, attaching a heat sink to the substrate and over the chip, and then encapsulating the heat sink and the chip (Figure 6).

It would have been obvious to one of ordinary skill in the art to use the heat sink of Lai in the combined invention of Booth and Applicant's admitted prior art because Lai teaches that this type of heat sink arrangement prevents resin flow during the molding process and also prevents the heat sink from causing a thermal compressive stress in the chip during cooling (2, 30+).

Conclusion

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (703)-305-3926.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone number where this application is assigned is (703)-308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703)-308-0956.

David A. Zarneke
May 31, 2003